FIG. 1

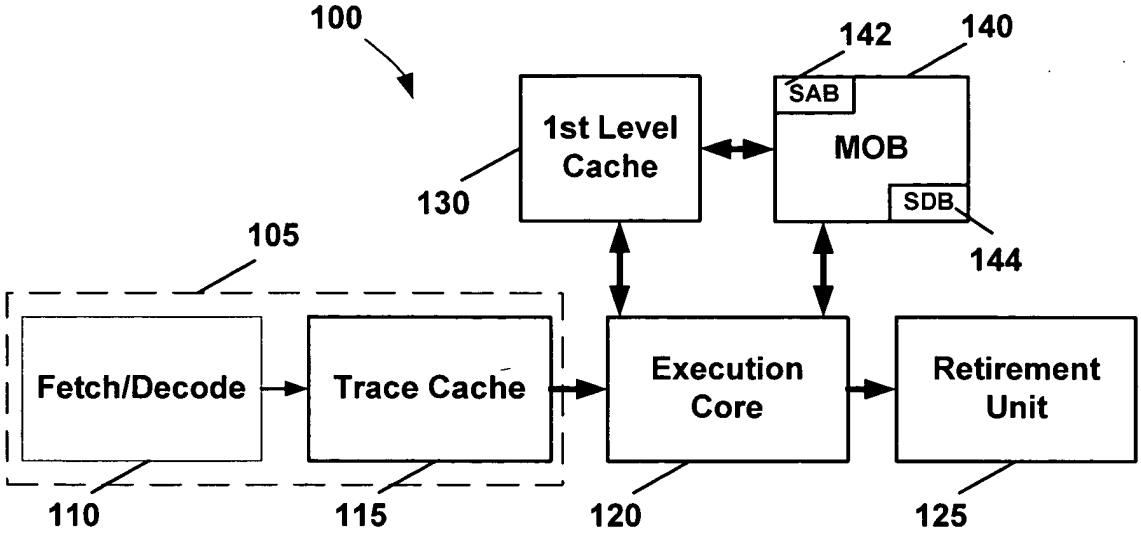

100
142
140
SAB
1st Level Cache
MOB
SDB
130
144
105
Fetch/Decode
Trace Cache
Execution Core
Retirement Unit
110
115
120
125

FIG. 2

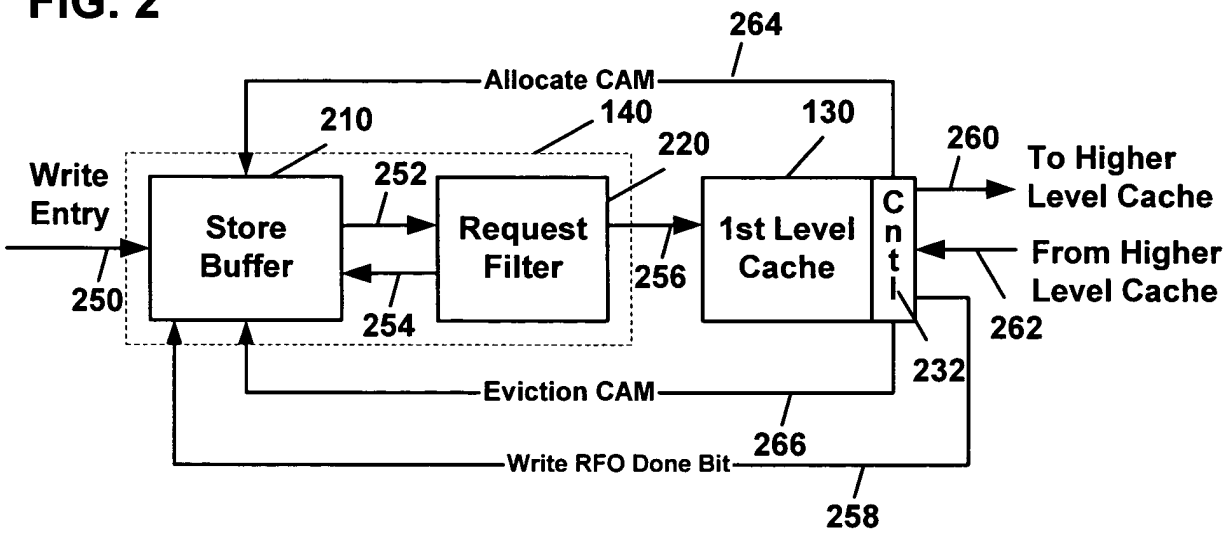

264
Allocate CAM
210
140
130
220
260
To Higher Level Cache
Write Entry
Store Buffer
252
Request Filter
1st Level Cache
Cntl
From Higher Level Cache
250
254
256
262
232
Eviction CAM
266
Write RFO Done Bit
258

FIG. 3

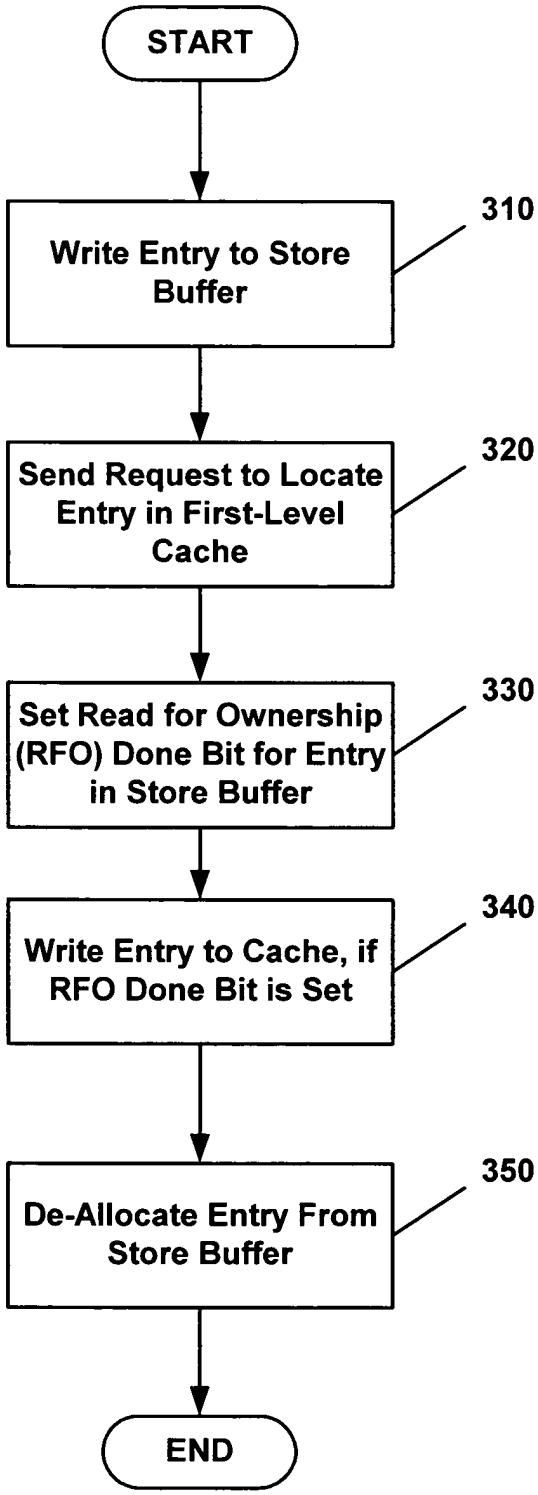

START
Write Entry to Store Buffer
310
Send Request to Locate Entry in First-Level Cache
320
Set Read for Ownership (RFO) Done Bit for Entry in Store Buffer
330
Write Entry to Cache, if RFO Done Bit is Set
340
De-Allocate Entry From Store Buffer
350
END

FIG. 4

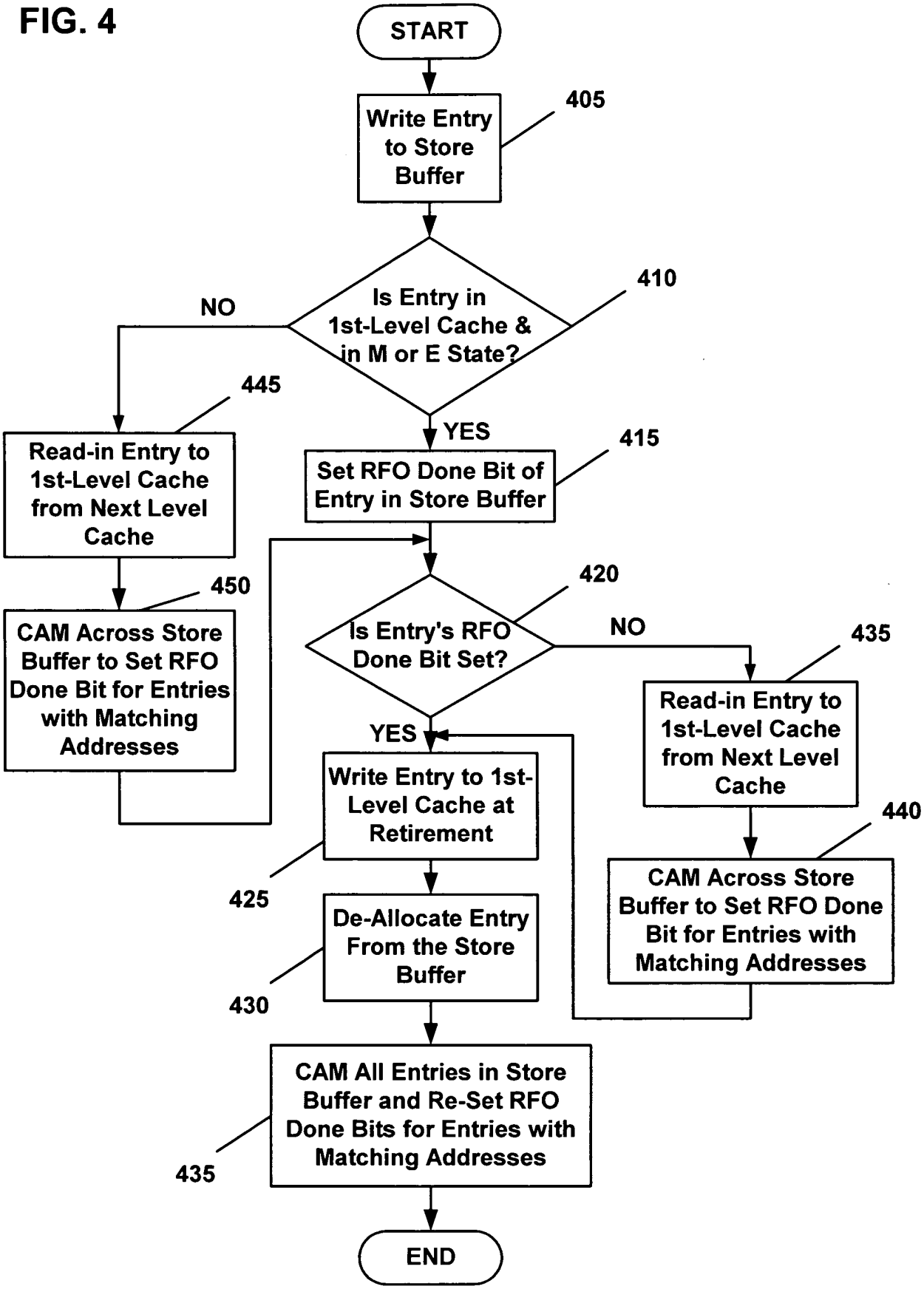
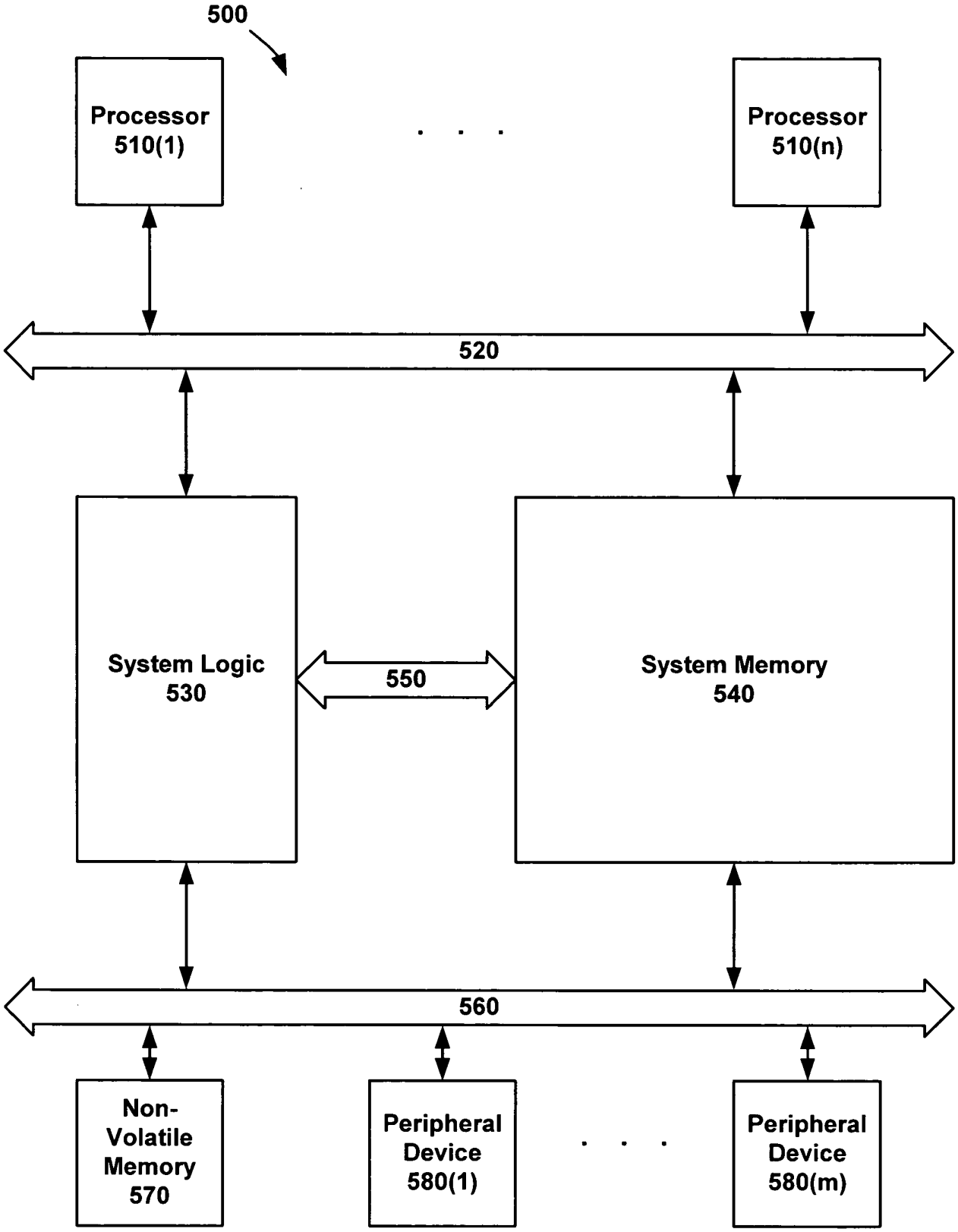

START
Write Entry to Store Buffer
405
Is Entry in 1st-Level Cache & in M or E State?
410
NO
YES
445
Read-in Entry to 1st-Level Cache from Next Level Cache
415
Set RFO Done Bit of Entry in Store Buffer
450
CAM Across Store Buffer to Set RFO Done Bit for Entries with Matching Addresses
420
Is Entry's RFO Done Bit Set?
NO
435
Read-in Entry to 1st-Level Cache from Next Level Cache
YES
Write Entry to 1st-Level Cache at Retirement
440
CAM Across Store Buffer to Set RFO Done Bit for Entries with Matching Addresses
425
De-Allocate Entry From the Store Buffer
430
CAM All Entries in Store Buffer and Re-Set RFO Done Bits for Entries with Matching Addresses
435
END

FIG. 5


500
Processor 510(1)
Processor 510(n)
520
System Logic 530
550
System Memory 540
560
Non-Volatile Memory 570
Peripheral Device 580(1)
Peripheral Device 580(m)